An Initial Implementation of a Direct Digital Synthesizer Module for Radar Applications

Julia Lanier
Department of Electrical and Computer Engineering
The University of Alabama
Tuscaloosa, AL, USA
jlanier@crimson.ua.edu

Ryan A. Taylor
Department of Electrical and Computer Engineering
The University of Alabama
Tuscaloosa, AL, USA
rtaylor@eng.ua.edu

Jie-Bang Yan
Departmet of Electrical and Computer Engineering
The University of Alabama
Tuscaloosa, AL, USA
jbyan@ua.edu

Abstract — **This paper presents an implementation of a DDS-based waveform synthesizer design using a wave table. The wave table contains 1024 8-bit points of a single period segment of a waveform. Using a constant access rate to read from the table, the frequency and shape of the waveform can be altered by either reading some points multiple times or skipping over some points. The waveform synthesizer was designed with Verilog HDL and implemented through the Altera DE1-SoC board. The program was designed to produce sawtooth, sine, square, and triangle waves in the frequency range of 100 Hz to 10 kHz. Future iterations of this design will implement frequency modulation for use in radar applications in the Remote Sensing Center at the University of Alabama.**

Keywords—waveform synthesis, direct digital synthesis, DDS, wave table, FPGA, hardware implementation

I. INTRODUCTION

Waveform synthesis is used for many different applications including instrumentation and communications. In regard to music, waveform synthesizers are used to manipulate frequencies of sound waves to either decrease high frequencies and produce a darker sound or increase low frequencies to produce a brighter sound. It is also used in radar applications to produce a variety of waveforms, leading to the ability to accomplish many things including target acquisition, tracking, and classification [1]. One method of producing waveforms with variable frequencies based off an existing waveform is called Direct Digital Synthesis (DDS). This method utilizes a phase accumulator and a look up table. This waveform synthesizer was designed using this DDS method. A DDS implementation of a waveform synthesizer can be used in a Frequency-Modulated Continuous-Wave (FM-CW) radar system. An FM-CW radar can precisely determine the range to a target by analyzing the frequency offset between two signals, known as the beat-frequency signal. These radars can be used for snow-depth measurement as well as soil-moisture measurements. The chirp generator of a DDS-based FM-CW radar can utilize a DDS, a frequency multiplier, and a frequency down-converter to generate a baseband chirp that is then fed into a frequency-multiplier subsection and mixed with a phase-locked loop (PLL) to generate the required chirp range. Figure 1 shows the block diagram of the chirp generator of a DDS-Based snow radar designed by Yan et al. in 2017 [2]. For a waveform synthesizer to be a practical addition to such a system, it must be able to generate frequency, and optionally amplitude, modulation over the course of a pulse, also known as a chirp. The future work section of this paper discusses the planned incorporation of this functionality.

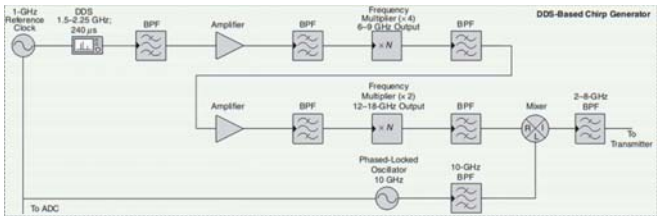

Figure 1. The system block diagram of a DDS-based chirp generator for an FM-CW radar [2].

Section two of this paper describes the waveform synthesizer design using Direct Digital Synthesis. In section three, we present some waveforms generated by the waveform synthesizer and discuss the practical applications of this design. Finally, section IV draws some conclusions and presents the future direction of this work.

II. WAVEFORM SYNTHESIZER

A wave table contains the data for a single period of a periodic wave. The output frequency of the waveform can be controlled by reading points from the wave table at a fixed frequency. Reading from a wave table at a fixed frequency is called the constant access rate method. Waveforms with variable frequencies can be produced by reading a single point multiple times to obtain a lowered frequency or skipping over some points to obtain a higher frequency. The output frequency can be found by simply diving the wave table sampling frequency

978-1-7281-0137-8/19/$31.00 ©2019 IEEE

by the number of points read. In this design, the wave table contained 1024 points and was sampled at 1 MHz. If every single point from the wave table is read the output frequency would be equal to roughly 977 Hz. If every fourth point from the wave table is read, 256 points, the output frequency would be equal to around 3.9 kHz. A phase accumulator is used to determine which points to read from the wave table.

Since the wave table is being read from at a fixed frequency, the address of the point to be read in the wave table needs to be quantified. This can be done with a phase accumulator. The phase accumulator begins at zero and is incremented by 1 bit every clock cycle. A number, called the step, is also added to the phase accumulator every clock cycle. If every point from the wave table should be read, the step would be 0. If every fourth point from the wave table should be read, the step would be 4. In other words, the higher the step, the fewer number of points are read from the wave table resulting in a higher output frequency. The phase accumulator also contains more bits than needed for the address. This is to allow for a wide range of output frequencies. In this design a 16-bit phase accumulator was implemented, and the 10 most significant bits were used as the address of the point to be read from the wave table. Equation 1 below shows how the number of points to be skipped (M), the fixed frequency used to read from the wave table (F_{sample}), and the n-bit accumulator (2^n) relate to one another.

$$F_{out} = \frac{M \times F_{sample}}{2^n} \quad (1)$$

Figure 2 shows the block diagram of how the wave table address is calculated, recreated from [3]. The system has seven inputs: the system clock, the desired output frequency, a reset, and four selection switches which correspond to the desired waveform shape. The four shape options for the waveform are a sawtooth, sine, square, or triangle wave.

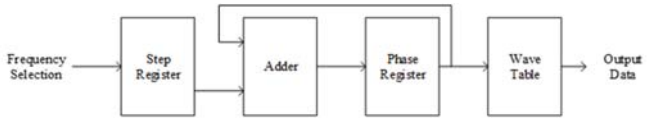

Figure 2. Block diagram of hardware necessary to compute the wave table address.

III. Results

The waveform synthesizer was implemented with the Altera DE1-SoC board. Each of the four waveform options were tested with frequencies of 100 Hz, 1 kHz, and 10 kHz. Figure 3 shows the sawtooth, sine, square, and triangle generated waveforms at the four frequencies respectively.

By default, as an output of the DE1-SoC board, the peak-to-peak voltage of these signals measure around 5.48 V. This corresponds to a power level of approximately 27.5 dBm, which is much greater than expected. Typical values for the output power level on chirp generators currently in use are in the range of 0-5 dBm. It remains to be seen how modulating the frequency will affect this system and that will be a focus of the next iteration of this implementation.

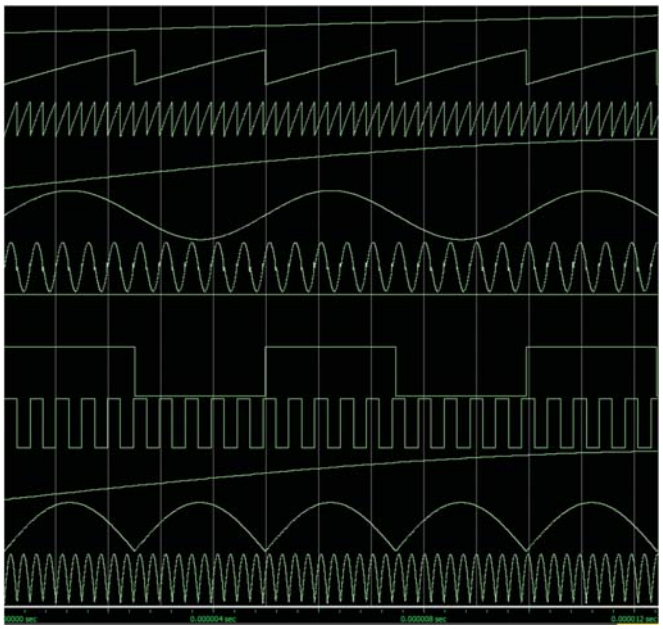

Figure 3. Generated sawtooth, sine, square, and triangle waveforms at 100 Hz, 1 kHz, and 10 kHz.

IV. Conclusions

A waveform synthesizer has been developed using a wave table and the Direct Digital Synthesis method. The sawtooth, sine, square, and triangle waveforms are generated using the phase accumulator to compute the address in which to read data from the wave table. The allowed output frequency range of the waveforms is 100 Hz to 10 kHz. The Verilog program for the waveform synthesizer is implemented on the Altera DE1-SoC board.

A. Future Work

As mentioned earlier, for this system to be of use in a radar chirp generator, it must be able to generate a frequency chirp. This is the focus of the next work on this design. There would be added benefit in being able to modulate the amplitude of the system as well and this will be explored in future iterations. Once the frequency-modulated chirp is synthesizable, the design will be prototyped and fabricated in silicon for testing.

References

[1] Adler, E., Viveiros, E., Ton, T., Kurtz, J., & Bartlett, M. (2002). Direct Digital Synthesis Applications for Radar Development. Proceedings International Radar Conference. Alexandria: IEEE.

[2] Yan, Jie-Bang, et al. "Airborne Measurements of Snow Thickness: Using Ultrawide-Band Frequency-Modulated-Continuous-Wave Radars." IEEE Geoscience and Remote Sensing Magazine, June 2017, pp. 57–76.

[3] Cole, C. (2014, October 24). EE324 Fundamentals of Digital Systems. Retrieved from https://eecs.wsu.edu/~ee324/Projects/Project4.pdf.